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FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
AGGARWAL, YOGESH K	
ART UNIT	**PAPER NUMBER**
2615	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/680,041	TAY, HIOK-NAM	
	Examiner	Art Unit	
	Yogesh K Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claims 1-59 have been considered but are moot in view of the new ground(s) of rejection.

2. Addition of new claims 60-65 is acknowledged.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim1-4, 8-10, 12-13, 15-18, 22-24, 26, 27, 29-40, 45-48, 50-59 and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heller et al. (US Patent # 6,396,539) in view of Tomura et al. (US Patent # 5,521,639) and in further view of Hiyama et al. (JP Patent # JP02000004403A).

[Claim 1]

Heller teaches a one-time programmable solid-state device (figure 2, element 10) (It is called one-time programmable because the memory 14 can be made of a fuse memory which can be programmed only once, See col. 4 lines 42-44) comprising a programmable memory unit (figure 2, element 14) embedded in a die within the one time programmable solid-state device (col. 3 lines 54-57) (The programmable memory 14 is embedded in a single chip 10); a driver circuit (figure 2, element 16) that programs the programmable memory unit (col. 4 lines 1-5); and an access circuit (figure 2, element 16) that enables access to the programmable memory unit (col. 4 lines 1-5, The applicant argues that the drive and the access circuits are two separate circuits. The Examiner respectfully

disagrees. The controller unit 16 has two separate buses for programming and accessing the memory 14, which means that it is writing and reading the memory separately. Therefore they are read as two different circuits performing two different functions).

Heller teaches storing the location of defective pixels in the memory (col. 8 lines 20-21) but fails to teach a driver circuit that programs the programmable memory unit with locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations.

However Tomura et al. teach that a frame memory 132 can be programmed to store a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations (col. 6 lines 46-54, figure 1a).

Therefore taking the combined teachings of Heller and Tomura, it would have been obvious to one skilled in the art at the time of the invention to have a programmable memory unit with locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations in order to

differentiate between the good and bad pixels. The benefit of doing so would be that less hardware is needed to differentiate between a good and a bad pixel.

Heller in view of Tomura fail to teach wherein the access circuit is configured to drive a row of the memory cells to ground that are to be read out. However Hiyama et al. teach a mode when the memory means 4 is reset before or after readout (Paragraph 17, figure 5 shows a row of memory cells).

Therefore taking the combined teachings of Heller, Tomura and Hiyama, it would have been obvious to one skilled in the art at the time of the invention to have a row of the memory cells to ground that are to be read out in order to have a picture signal in a high speed mode. The benefit of doing so would be to have a picture being read in a high-speed mode as taught in Hiyama (Abstract).

[Claim 2]

Heller teaches that the programmable memory unit includes a number of memory cells having a gate (col. 4 lines 36-39, col. 4 lines 49-51)[CMOS has a gate].

[Claim 3]

Heller teaches that the memory cells are arranged in a two-dimensional array having a number of rows of memory cells and a number of columns of memory cells (Figure 2 discloses a programmable memory 14 arranged in a two-dimensional array having a number of rows and columns]

[Claim 4]

Heller teaches that the number of rows of memory cells is equal to a predetermined number, and the number columns of memory cells is equal to the predetermined number [It is inherent that the number of rows and columns is equal to a predetermined number].

[Claims 8-10]

Heller teaches that a code is stored in the programmable memory unit (col. 4 lines 49-57) [The security/identification values include a code, serial number or a product identifier].

[Claim 12]

Heller teaches that the number of memory cells contains an address of at least one defective pixel that is located in an imaging device on the die of the one time programmable solid-state device (col. 8 lines 21-22 figure 5: step 64).

[Claim 13]

Heller teaches that the at least one memory cell of the number of memory cells is permanently encoded (col. 6 lines 17-22)[Using fuse memory to program identification information makes it permanently encoded].

[Claim 15]

Heller teaches that the driver circuit and access circuit are embedded in the die (col. 3 lines 54-57, col. 4 lines 1-5)[The programmable memory 14 is embedded in a single chip 10. The driver circuit and access contained in the controller unit 16 are both contained in the same die];

[Claims 16-18, 22-24,26,27]

These claims correspond to claims 2-4, 8-10,12,13. Therefore claims 16-18, 22-24,26,27 have been analyzed and rejected based upon the claims 2-4, 8-10,12,13 respectively.

[Claim 29]

Heller teaches a one-time programmable solid-state device comprising writing, with a driver circuit (figure 2: 16), to a programmable memory unit (figure 2: 14) embedded in a die within the programmable solid-state device (col. 4 lines 1-5); and

accessing, with an access circuit (figure 2: 16), the one time programmable solid-state device (col. 4 lines 1-5(col. 4 lines 1-5, The applicant argues that the drive and the access circuits are two separate circuits. The Examiner respectfully disagrees. The controller unit 16 has two separate buses for programming and accessing the memory 14, which means that it is writing and reading the memory separately. Therefore they are read as two different circuits performing two different functions).

Heller teaches storing the location of defective pixels in the memory (col. 8 lines 20-21) but fails to teach a driver circuit that programs the programmable memory unit with locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations.

However Tomura et al. teach that a frame memory 132 can be programmed to store a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations (col. 6 lines 46-54, figure 1a).

Therefore taking the combined teachings of Heller and Tomura, it would have been obvious to one skilled in the art at the time of the invention to have a programmable memory unit with locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second

logic value represents a defective pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations in order to differentiate between the good and bad pixels. The benefit of doing so would be that less hardware is needed to differentiate between a good and a bad pixel.

Heller in view of Tomura fail to teach wherein the access circuit is configured to drive a row of the memory cells to ground that are to be read out. However Hiyama et al. teach a mode when the memory means 4 is reset before or after readout (Paragraph 17, figure 5 shows a row of memory cells).

Therefore taking the combined teachings of Heller, Tomura and Hiyama, it would have been obvious to one skilled in the art at the time of the invention to have a row of the memory cells to ground that are to be read out in order to have a picture signal in a high speed mode. The benefit of doing so would be to have a picture being read in a high-speed mode as taught in Hiyama (Abstract).

[Claim 30]

Heller teaches that the programmable solid-state device is a solid-state imaging device (col. 3 lines 54-57. figure 2: 10).

[Claim 31]

Heller teaches that further includes identifying a defective pixel within the solid-state imaging device (col. 8 lines 21-22 figure 5: step 64).

[Claim 32]

Heller teaches that the driver circuit and access circuit are embedded in the die (col. 4 lines 1-4 figure 2: 10 and 16)[The controller unit 16 contains both the access and driver unit and is contained on the same chip 10]

[Claim 33]

Heller teaches that the programmable solid-state device is a solid-state imaging device (col. 3 lines 54-57. figure 2: 10).

[Claims 34-36]

Heller teaches writing further includes storing a code in the programmable memory unit (col. 4 lines 49-57) [The security/identification values include a code, serial number or a product identifier].

[Claim 37]

Heller teaches a method of data storage comprising identifying an address of a defective pixel in a photo-sensor having a plurality of pixels arranged in a two-dimensional array in a die within a programmable solid-state imaging device and storing the address in a programmable memory unit that is embedded in the die of the solid-state imaging device (col. 7 lines 49-57).

Heller teaches storing the location of defective pixels in the memory (col. 8 lines 20-21) but fails to teach a driver circuit that programs the programmable memory unit with locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations.

However Tomura et al. teach that a frame memory 132 can be programmed to store a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective

pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations (col. 6 lines 46-54, figure 1a).

Therefore taking the combined teachings of Heller and Tomura, it would have been obvious to one skilled in the art at the time of the invention to have a programmable memory unit with locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations in order to differentiate between the good and bad pixels. The benefit of doing so would be that less hardware is needed to differentiate between a good and a bad pixel.

Heller in view of Tomura fail to teach wherein the access circuit is configured to drive a row of the memory cells to ground that are to be read out. However Hiyama et al. teach a mode when the memory means 4 is reset before or after readout (Paragraph 17, figure 5 shows a row of memory cells).

Therefore taking the combined teachings of Heller, Tomura and Hiyama, it would have been obvious to one skilled in the art at the time of the invention to have a row of the memory cells to ground that are to be read out in order to have a picture signal in a high speed mode. The benefit of doing so would be to have a picture being read in a high-speed mode as taught in Hiyama (Abstract).

[Claim 38]

The method of claim 37 wherein identifying includes identifying a row and a column that corresponds to the defective pixel in the photo-sensor (col. 7 lines 49-57)[It is inherent

that when the location of a defective pixel is identified both the row and column of that pixel has to be identified].

[Claim 39]

The method of claim 38 wherein storing includes permanently encoding the address of the defective pixel in the programmable memory unit [If a fuse memory is used as explained above then the address of the defective pixel location is permanently encoded or programmed].

[Claim 40]

The method of claim 39 wherein storing further includes permanently encoding the address into a row having a plurality of transistors in the programmable memory unit, where each transistor in the plurality of transistors has a gate (col. 4 lines 36-39, col. 4 lines 49-51)[Permanently encoding is read as programming the CMOS memory array with an address wherein each CMOS has a gate].

[Claims 45-48, 50]

Claims 45-48, 50 are apparatus claims corresponding to method claims 1-4 and 15 respectively. Therefore they have been analyzed and rejected based upon method claims 1-4 and 15.

[Claims 51-56]

Claims 51-56 are apparatus claims corresponding to method claims 29,30,34-36,32 respectively. Therefore they have been analyzed and rejected based upon method claims 29,30,34-36,32.

[Claims 57-59]

Claims 57-59 these are apparatus claims corresponding to method claims 37-39 respectively. Therefore they have been analyzed and rejected based upon method claims 37-39.

[Claim 65]

Heller teaches a one-time programmable solid-state device (figure 2, element 10) (It is called one-time programmable because the memory 14 can be made of a fuse memory which can be programmed only once, See col. 4 lines 42-44) comprising a programmable memory unit (figure 2, element 14) embedded in a die within the one time programmable solid-state device (col. 3 lines 54-57) (The programmable memory 14 is embedded in a single chip 10); a means for driving configured to program the programmable memory unit (figure 2, element 16, col. 4 lines 1-5). Tomura et al. teach that a frame memory 132 can be programmed to store a first logic value or a second logic value, wherein the first logic value represents a good pixel at the corresponding location and the second logic value represents a defective pixel at the corresponding location, and wherein the individual memory cells are associated with respective pixel locations (col. 6 lines 46-54, figure 1a).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 11, 25 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heller et al. (US Patent # 6,396,539), Tomura et al. (US Patent # 5,521,639),

Hiyama et al. (JP Patent # JP02000004403A) and in further view of Banham et al. (US Patent # 6,141,453).

[Claims 11]

Heller in view of Tomura and Hiyama teach the limitations of claim 2 but fails to teach ".... wherein the solid-state device is an application specific integrated circuit (ASIC) having at least one predetermined configuration value in the programmable memory unit." However Banham discloses that it is well known and used in the art to have a solid-state device is an application specific integrated circuit (ASIC) having at least one predetermined configuration value in the programmable memory unit (col. 7 lines 5-10 figure 6: 601)[The device disclosed can be implemented as a memory which is programmable and is an ASIC]. Therefore taking the combined teachings of Heller, Tomura, Hiyama and Banham it would have been obvious to one skilled in the art at the time of the invention to have a solid-state device which is an application specific integrated circuit (ASIC) having at least one predetermined configuration value in the programmable memory unit. Doing so would reduce the cost of manufacture, as ASICs can be mass-produced to have a smaller cost.

[Claim 25]

Claim 25 corresponds to claim 11. Therefore it has been analyzed and rejected based upon the claim 11.

[Claim 49]

Claim 49 is an apparatus claim corresponding to method claim 11. Therefore it has been analyzed and rejected based upon method claim 11.

7. Claims 5-7, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heller et al. (US Patent # 6,396,539), Tomura et al. (US Patent # 5,521,639), Hiyama et al. (JP Patent # JP02000004403A) and in further view of Forbes et al. (US PG-PUB # 2002/0001219).

[Claim 5]

Heller in view of Tomura and Hiyama teach the limitations of claim 2 but fails to teach ".... wherein each memory cell in the number of memory cells is a capacitor". However Forbes discloses that it is well known and used in the art to have a memory cell formed of a capacitor (Paragraph 0054, figure 2(a): 118 and 100). [The reference discloses that the memory 100 has a capacitor 118 and can be used in a CMOS technology]. Therefore taking the combined teachings of Heller, Tomura, Hiyama and Forbes it would have been obvious to one skilled in the art at the time of the invention to have a memory cell formed of a capacitor. Doing so would allow the overall area of the memory to be smaller because the surface area of the capacitor is small as compared to the gate electrode as taught in Forbes (Paragraph 0055 lines 4-7).

[Claims 6 and 7]

Heller in view of Tomura and Hiyama teach the limitations of claim 2 but fails to teach ".... wherein each memory cell in the number of memory cells is a transistor and wherein the transistor is a FET. However Forbes discloses that it is well known and used in the art to have a memory cell formed of a transistor and wherein the transistor is a FET (Paragraph 0054, figure 2(a): 114 and 100). [The reference discloses in figure 2(a) that the memory 100 has a transistor 114, which is a FET and can be used in a CMOS technology]. Therefore taking the combined teachings of Heller, Tomura, Hiyama and

Forbes it would have been obvious to one skilled in the art at the time of the invention to have a memory cell formed of a transistor and wherein the transistor is a FET. Doing so would allow the memory cell to be programmed with a voltage as low as +/- 5V, which is consistent with CMOS technology as taught in Forbes (Paragraph 0054).

[Claims 19-21]

Claims 19-21 correspond to claims 5-7. Therefore claims 19-21 have been analyzed and rejected based upon the claims 5-7 respectively.

8. Claims 14, 28, 41, 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heller et al. (US Patent # 6,396,539), Tomura et al. (US Patent # 5,521,639), Hiyama et al. (JP Patent # JP02000004403A) and in further view of Haroun et al. (US Patent # 6,532,514).

[Claims 14, 28 and 41]

Heller in view of Tomura and Hiyama teach the limitations of claim 13, 27 and 40 but fail to teach "…. wherein storing further includes breaking down the gate on each transistor in the plurality of transistors that corresponds to a logic 1 in the address". However Haroun discloses that it is well known and used in the art to have logic one in the memory by breaking down the gate (col. 3 lines 11-19). Therefore taking the combined teachings of Heller, Tomura, Hiyama and Haroun it would have been obvious to one skilled in the art at the time of the invention to have logic one in the memory by breaking down the gate. Doing so would allow to easily identifying the rest of the transistors, which have logic zero making the process faster.

[Claim 42]

The method of claim 41 further includes accessing the address stored in the programmable memory unit (Heller, col. 8 lines 39-50).

9. Claims 43, 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heller et al. (US Patent # 6,396,539), Tomura et al. (US Patent # 5,521,639), Hiyama et al. (JP Patent # JP02000004403A), Haroun et al. (US Patent # 6,532,514) and in further view of Michiyama (US Patent # 5,410,511).

[Claim 43]

Heller in view of Tomura, Hiyama and Haroun teaches the limitations of claim 42 but fails to teach ".... wherein accessing further includes detecting a leakage current flowing through the gate oxide of at least one of the transistors". However Michiyama discloses that it is well known and used in the art to detect a leakage current flowing through the gate oxide of at least one of the transistors (col. 8 lines 35-39). Therefore taking the combined teachings of Heller, Tomura, Hiyama, Haroun and Michiyama it would have been obvious to one skilled in the art at the time of the invention detect a leakage current flowing through the gate oxide of at least one of the transistors. Doing so would allow reading the information in the flash memory as taught in Michiyama (col. 8 lines 35-39).

[Claim 44]

The method of claim 43 wherein accessing further includes amplifying the detected leakage current (col. 8 lines 35-39).

10. Claims 60-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heller et al. (US Patent # 6,396,539), Tomura et al. (US Patent # 5,521,639), Hiyama et al. (JP Patent # JP02000004403A) and in further view of Lesea et al. (US Patent # 6,275,191).

[Claims 60-64]

Heller in view of Tomura and Hiyama teach the limitations of claim 1, 29, 37, 45, and 51 but fail to teach "driving an inverter to ground corresponding to a row of memory cells that are to be programmed". However Lesea et al. teaches that a memory cell 149 is programmed to output a digital logic high so that an N channel transistor 148 is conductive and couples input 133 of inverter 130 to ground (col. 6 lines 7-10, figure 4 shows a row of two receivers 115, 116 which contain memory cells 149 and inverters 130 corresponding to those memory cells). Therefore taking the combined teachings of Heller, Tomura, Hiyama and Lesea, it would have been obvious to one skilled in the art at the time of the invention to have driven an inverter to ground corresponding to a row of memory cells that are to be programmed in order to disable the whole circuit in which memory cell is contained. The benefit of doing so would be to disable the whole circuit in which the memory cell is contained as taught in Lesea (col. 6 lines 7-10).

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K Aggarwal whose telephone number is (703) 305-0346. The examiner can normally be reached on M-F 9:00AM-5:30PM.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
September 15, 2004

TUAN HO
PRIMARY EXAMINER